ABSTRACT

Power consumption in dynamic logic circuit increases with frequency of operation, voltage swing and dynamic node capacitance. Wide-fan-in OR Gates is being widely used in semiconductor memories have large dynamic node capacitance which increases delay. The Dominos Logic consists of Pre-charge and Evaluation network. The parallel connection used in the evaluation network leads to memory leakage current in decoders. This leakage current changes the voltage of the dynamic node during evaluation phase to decrease the noise immunity.

In CMOS circuits, power dissipation is obtained by reducing the threshold voltage due to voltage scaling. Voltage scaling leads to increase in gate leakage current and sub threshold leakage current or static power dissipation. In this proposed work, DMG TFET based different type of LECTOR, GALEOR, SN-LECTOR and SP-LECTOR are introduced for designing a low power CMOS circuits. The proposed designs consist of p-type and n-type transistors which introduced between the pull up network and pull down network. The significant feature of the proposed work is to reduce the active power consumption resulting in better leakage reduction compared to the other technique. Further Without increasing the dynamic power, these techniques do not affect the switching power. Wide-fan-in OR gates can be designed using 16nm V2.1 HP Predictive Technology Model (PTM) (except LECTOR, GALEOR, SN-LECTOR and SP-LECTOR). For designing LECTOR, GALEOR, SN-LECTOR and SP-LECTOR a DMG TFET is designed using TCAD simulation software. In this model, the active and standby power consumption is observed at 110°C temperature. Performance can be increased due to decreasing the output voltage swing.

First, Tunnel Field Effect Transistor (TFET) provides a deeper examination in the scaling limitations of MOSFET. TFET has superior properties, here Sub threshold Swing (SS) is smaller than 60mv/decade at room temperature and also TFET shows small leakage current in the range of femto amperes. In this work, a new 2- Dimensional analytical model for dual material gate tunnel field effect transistor (DMG-TFET) is proposed. The parabolic approximation technique is used to solve the 2D Poisson equation with suitable boundary conditions. Analytical modelling of parameters like threshold voltage, surface potential and electric field are derived. The proposed DMG TFET is being used in Domino logic which provides higher efficiency to prevent short channel effects (SCE). DMG TFET shows a significant on-current improvement and reduction in SCE. The mathematical model of the proposed DMG TFET has been verified by comparing the analytical results with TCAD simulation.

Second, using proposed DMG TFET the following networks has been designed and calculates the estimation of resistance in LECTOR, GALEOR, SN-LECTOR and SP-LECTOR networks. Simulation results were obtained from Tanner V-15 with the help of designed dual material gate tunnel field effect transistor (DMG TFET) with first work function as gold and second work function as titanium.

Finally, by using the DMG TFET based LECTOR, GALEOR, SN-LECTOR and SP-LECTOR in dominos circuits, the power consumption is optimized with little increases in area i.e. two transistors in LECTOR and GALEOR, three transistors in SN-LECTOR and SP-LECTOR. The performance of proposed DMG TFET based LECTOR, GALEOR,SN-LECTOR and SP-LECTOR domino circuits in terms of power consumption is being analysed in this work.